region for which performance such as that described above is required, its performance and yield are expected to be significantly increased.

[0151] In the heterojunction type compound semiconductor field effect transistor according to the present embodiment, the GaAs contact underlayer **17** or the InGaAs contact underlayer **17** is exposed from the bottom of the wide recess opening **5**. This prevents the failure to form the narrow recess opening **10** as occurs in the prior art. As a result, the yield can be increased.

[0152] Furthermore, as in the case with the second embodiment, the recess stopper layer **50** can be made thinner than the contact underlayer **17**.

[0153] [Variation 2]

[0154] **FIG. 25** is a sectional view of the structure of a variation of the heterojunction type compound semiconductor field effect transistors according to the fourth embodiment of the present invention. As shown in **FIG. 25**, an undoped GaAs layer is stacked on the semi-insulating GaAs substrate **11** as the buffer layer **12**. Furthermore, the n-$Al_{0.2}Ga_{0.8}As$ layer is stacked on the buffer layer **12** as the lower electron supply layer **13**. The i-$Al_{0.2}Ga_{0.8}As$ layer is formed on the electron supply layer **13** as the lower spacer layer (not shown). The i-$In_{0.15}Ga_{0.85}As$ layer is formed on the lower spacer layer as the channel layer **14**. The i-$Al_{0.2}Ga_{0.8}As$ layer is formed on the channel layer **14** as the upper spacer layer (not shown). The n-$Al_{0.2}Ga_{0.8}As$ layer is formed on the upper spacer layer as the upper electro supply layer **15**. On the electro supply layer **15**, the i-$In_{0.48}Ga_{0.52}P$ layer as the electric field strength reducing layer **16**, the n-GaAs layer as the contact underlayer **17**, and the low-resistance $n^+$-GaAs layer as the contact overlayer **18** are sequentially stacked.

[0155] The wide recess opening **5** is formed in the contact overlayer **18** so as to penetrate this layer **18**. The narrow recess opening **10** narrower than the wide recess opening is formed inside the wide recess opening **5** so as to penetrate the contact underlayer **17**. That is, the heterojunction type compound semiconductor field effect transistor shown in **FIG. 25** has a double recess structure composed of the wide recess opening **5** and the narrow recess opening **10**.

[0156] Moreover, the gate electrode **22** composed of, for example, Al is formed on the surface of the electric field strength reducing layer **16** exposed from the bottom of the narrow recess opening **10**. The source electrode **20** and drain electrode **21**, each composed of, for example, AuCe/Ni/Au, are formed on the contact overlayer **18** so as to sandwich the wide recess opening **5** between them.

[0157] As described above, the contact underlayer **17**, forming the narrow recess opening **10**, contains GaAs doped with n type impurities. The contact overlayer **18**, forming the wide recess opening **5**, also contains GaAs doped with a higher concentration of n type impurities. Moreover, the electric field strength reducing layer **16** is formed of intrinsic InGaP.

[0158] The present embodiment differs from Variation 1 in that the gate electrode **22** is formed on the surface of the electric field strength reducing layer **16** exposed from the bottom of the narrow recess opening **10**.

[0159] Accordingly, for a reason similar to that in the third embodiment, the gate electrode **22** is connected to the surface of the electric field strength reducing layer **16**, having a low carrier trap concentration. Improved reliability and performance can thus be achieved compared to the conventional heterojunction type compound semiconductor field effect transistor shown in **FIG. 1**.

[0160] Basic operations are similar to those of Variation 1, and their detailed description is thus omitted.

[0161] Basically, this method first executes steps similar to those shown in FIGS. **3** to **10**. However, this method differs from the first embodiment in that when the wide recess opening **5** is formed in the contact overlayer **18** in the steps shown in **FIGS. 5 and 6**, an etching operation must be accurately preformed by using an $H_3PO_4$-based etchant and controlling time, temperature, or the like.

[0162] Subsequently, steps such as those shown in FIGS. **7** to **10** are executed to obtain an intermediate structure such as that shown in **FIG. 10**.

[0163] Then, using an insulating film formed with a pattern used to form the narrow recess opening **10**, the contact underlayer **17** is wet-etched using an $H_3PO_4$-based etchant composed of, for example, $H_3PO_4$, $H_2O_2$, and $H_2O$ in the ratio of 3:1:50. The narrow recess opening **10** is thus formed so as to penetrate the contact underlayer **17**. At this time, the $H_3PO_4$-based etchant does not substantially etch InGaP. Accordingly, once the surface of the i-$In_{0.48}Ga_{0.52}P$ layer, the electric field strength reducing layer **16**, is exposed, the recess etching penetrating the contact underlayer **17** is substantially stopped.

[0164] Then, the gate electrode **22** composed of, for example, Ti/Pt/Au or Ti/Al or Al is formed on the surface of the upper electron supply layer **15** exposed from the bottom of the narrow recess opening **10**, using, for example, the liftoff method. Alternatively, the gate electrode **22** may be formed of a high-melting-point metal.

[0165] Finally, the protective film **42** composed of, for example, SiN is formed all over the surface of the structure to complete a heterojunction type semiconductor field effect transistor.

[0166] As described above, in the step of forming the narrow recess opening **10**, the $H_3PO_4$-based etchant etches the i-$In_{0.48}Ga_{0.52}P$ layer, the electric field strength reducing layer **16**, very slowly. Thus, once the surface of the electric field strength reducing layer **16** is exposed, the recess etching penetrating the n type contact underlayer **17** is substantially stopped. Accordingly, the electric field strength reducing layer **16** is effective in reducing electric fields that may be generated near the gate electrode **22**, and also functions as an etching stopper during the manufacturing process. This enables a high etching accuracy to be maintained during the manufacturing process, thus making use of the advantages of the double recess structure.

[0167] Moreover, compared to the first embodiment, it is possible to omit the step of etching the electric field strength reducing layer **16**. Manufacturing costs can thus be reduced.

[0168] In the above embodiments, the InGaP layer cannot be replaced with the AlGaAs layer. A dry etching technique using a gas containing a F (fluorine)-based gas is known to be able to appropriately etch the GaAs or InGaAs layer so